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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,130	10/17/2001	Shimman Patel	990530	5529

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 09/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/981,130	PATEL ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/17/01; 11/29/02; 06/09/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/29/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1-18 are objected to because of the following informalities:

Re claim 1, the applicant is advised to remove the close parentheses ")" in line 3; to change the phrase "A and B = M-A" in line 4 as "A and B wherein B = M – A" for clarification; and to change the phrase "(A modulo J)" in line 5 as "A modulo J (A mod J)" for clarification.

Re claim 2, the applicant is advised to change the phrase "multiplexer M1" in line 1 as "multiplexer (M1)" for clarification.

Re claim 4, the applicant is advised to change the phrase "multiplexer M2" in line 2 as "multiplexer (M2)" for clarification.

Re claim 5, the applicant is advised to change the phrase "adder A1" in line 1 as "adder (A1)" for clarification and change the phrase "($\alpha_1 C_1$)" in line 2 as "$\alpha_1 C_1$" for clarification.

Re claim 6, the applicant is advised to change the phrase "multiplexer M4" in line 1 as "multiplexer (M4)" for clarification and change the phrase "(M' < J)" in line 2 as "M' < J" for clarification.

Re claims 8-9, the applicant is advised to change the phrase "multiplexer M3" in line 1 as "multiplexer (M3)" for clarification.

In addition, claims 11-18 have similar objections and the applicant is advised to review and correct the similar objections as listed above.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 1, the limitation "the number" in line 2 lacks antecedence basis. For examination purposes, the examiner considers the limitation as a number of digits in M. In addition, the limitation "feeding M' back to the first means to evaluate M' modulo J" in lines 7-8 is unclear because the first means is unknown and the claim purpose is to evaluate M modulo J, not M' modulo J. For examination purposes, the examiner considers the limitation as "feeding M', as M, back to the first circuit and repeat to evaluate M modulo J". Claims 10-11 have the same problems.

Re claim 2, it is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: B_N, B_i, and limitations cited in claim 1. This claim lacks or omits essential structural cooperative relationships between B_N, B_i and the evaluation of first, second, third, and fourth circuits. Neither

claim 1 nor claim 2 disclose the use or structure of B_N and B_i. Claims 3, 5, 12-13, and 15 have the similar problem.

Re claim 5, the limitation "B_i and $(\alpha_1 C_1)$" in line 2 lacks antecedence basis. For examination purposes, the examiner considers the limitation "B_i and $(\alpha_1 C_1)$" as any number. Claim 15 has the similar problem.

Re claim 7, the limitation "fifth circuit" in line 7 is indefinite because it does not point out to any particular circuit or particular function for this fifth circuit for ensuring convergence. For examination purposes, the examiner disregards the limitation cited in this claim. Claim 17 has the similar problem.

Thus, claims 4, 6, 8-9, 14, 16, and 18 also rejected for being dependent on the rejected base claims 1 and 11.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 11-17 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 11-17 clearly recite a method for evaluating a modulo factor according to a mathematic algorithm. In order for such a claimed method, computer-related process, or a claimed non-specified apparatus implementing the underlined process to be statutory, the claims must include either a step or means that results in a physical transformation outside the computer or a limitation to a practical application. However, it is clear from

the claims that the claims merely recite step or non-specific means for data computation and manipulation in performing a mathematical function. The input is a set of numbers and output is also a set of numbers. The claims fail to recite any step or means that results in a physical transformation outside the computer, that includes a limitation to a practical application, or that requires a specific computer to implement the claimed process. Therefore, claims 11-17 are clearly directed to a non-statutory subject matter.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 5-7, 10-13, and 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Takenaka et al. (U.S. 5,499,299).

Re claim 1, Takenaka et al. disclose in Figure 2 a system for evaluating M modulo J, where J is an integer and M is an integer N expressed in binary form, where alpha, is 0 or 1, and N+1 is the number of digits in a binary word (abstract wherein T mod N) comprising: a first circuit (1) for decomposing M into two integers A and B = M - A; a second circuit (2 and col. 8 lines 32-35) for evaluating (A modulo J); a third circuit (3) for evaluating M' = (A modulo J) + B; and a fourth circuit for outputting M' (4) or feeding M' back to the first means to evaluate M' modulo J (n times loop).

Re claim 2, Takenaka et al. further disclose in Figure 2 the first circuit includes a multiplexer M1passes Bn to the second circuit on a first iteration and passes Bi on all subsequent iterations, where i is an iteration counter starting with N and counting down (Figure 2 with n times loop).

Re claim 3, Takenaka et al. further disclose in Figure 2 the second circuit includes a look-up table that stores C = 2 modulo J for i = 0 to N (col. 8 lines 30-37).

Re claim 5, Takenaka et al. further disclose in Figure 2 the third circuit (3) includes an adder (3) whose inputs are B (output direct from T register) and (alpha*C) (output of 5) and which passes its output M' = Bi + (alpha*C) to the fourth circuit (4).

Re claim 6, Takenaka et al. further disclose in Figure 2 the fourth circuit includes a multiplexer M4 that passes M' as a final output if (M' < J) (output of 4); otherwise i is set to i-l, and M' is fed back to the first circuit (n times loop).

Re claim 7, Takenaka et al. further disclose in Figure 2 the circuit further includes fifth circuit for ensuring convergence (18-20).

Re claim 10, it is a system claim of claim 1. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 11, it is a method claim of claim 1. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 12, it is a method claim of claim 2. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 13, it is a method claim of claim 3. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 15, it is a method claim of claim 5. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 16, it is a method claim of claim 6. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 17, it is a method claim of claim 7. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Allowable Subject Matter

8. Claims 4 and 8-9 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,763,365 to Chen et al. disclose a hardware implementation for modular multiplication using a plurality of almost entirely identical processor elements.

b. U.S. Patent No. 4,989,171 to Hollmann discloses a data processing method and apparatus for calculating a multiplicatively inverted element of a finite field.

c. U.S. Patent No. 6,763,366 to Hars et al. disclose a method for calculating arithmetic inverse over finite fields for use in cryptography.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

September 1, 2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
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